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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/768,851	01/23/2001	Kenichi Sanpei	450100-02949	3091

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EXAMINER	
MISLEH, JUSTIN P	

ART UNIT	PAPER NUMBER
2622	

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12/03/2008	PAPER

Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Office Action Summary	Application No.	Applicant(s)	
	09/768,851	SANPEI, KENICHI	
	Examiner	Art Unit	
	JUSTIN P. MISLEH	2622	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE *3* MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *29 September 2008*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-20* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-20* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

Continued Examination Under 37 CFR 1.114

1. A request for continued examination under 37 CFR 1.114, including the fee set forth in 37 CFR 1.17(e), was filed in this application after final rejection. Since this application is eligible for continued examination under 37 CFR 1.114, and the fee set forth in 37 CFR 1.17(e) has been timely paid, the finality of the previous Office action has been withdrawn pursuant to 37 CFR 1.114. Applicant's submission filed on September 29, 2008 has been entered.

Response to Arguments

2. Applicant's arguments filed September 29, 2008 have been fully considered but they are not persuasive.

3. Applicant argues, "Indeed, claim 1 recites a frequency dividing means that generates and outputs a normal vertical clock for reading out the image signals and a high speed clock having a higher frequency than that of the normal vertical clock. None of the references replied upon by the Office Action discloses or teaches the above-identified features of claim 1."

4. The Examiner respectfully disagrees with Applicant's position. Nishizawa et al. give clear indication that the clock pulse generator (CPG) is a frequency dividing means that generates and outputs a normal vertical clock for reading out the image signals and a high speed clock having a higher frequency than that of the normal vertical clock. See column 7 (lines 13-26). For this reason, the rejection will be maintained.

Claim Rejections - 35 USC § 103

5. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

6. **Claims 1 – 20** are rejected under 35 U.S.C. 103(a) as being unpatentable over Parulski et al. (US 5,668,597) in view of Kijima et al. (US 6,700,610 B1) in further view of Nishizawa et al. (US 4,841,369).

NOTE: The Examiner notes that Claims 1 and 6 appear to be corresponding apparatus and method claims, respectively; the Examiner further notes that Claims 11 and 16 also appear to be corresponding apparatus and method claims, respectively. Accordingly, Claims 1 and 6 will be rejected together and Clams 11 and 16 will be rejected together.

Moreover, Claims 2, 7, 12, and 17 are substantially and substantively the same; accordingly, they will be rejected together. Further, Claims 3, 8, 13, and 18 are substantially and substantively the same; accordingly, they will be rejected together. Further, Claims 4, 9, 14, and 19 are substantially and substantively the same; accordingly, they will be rejected together. Further, Claims 5, 10, 15, and 20 are substantially and substantively the same; accordingly, they will be rejected together.

7. For **Claims 1 and 6**, Parulski et al. disclose, as shown in figures 1, 4, 5, 8, and 9 and as stated in columns 4 (lines 49 – 59), 5 (lines 54 – 67), 6 (lines 1 – 14, 19 – 22, and 26 – 33), 8 (lines 6 – 67), and 9 (lines 1 – 8), an image photographing apparatus and method of operating thereof for photographing a still image, comprising:

a scanning imaging device (sensor 20; see figures 1 and 4) for generating image signals; and

a control means (processor section 35 and timing control section 27; see figure 1) for using the image signals generated by said imaging device (sensor 20) to adjust the still image during at least one control period before photographing (As shown in figure 9, the claimed "photographing" is in the step "Integrate Final Image"; the claimed "adjust the still image" corresponds to all the steps prior to the "Integrate Final Image Step"; one iteration of the "Focus Acceptable" loop corresponds to the claimed "at least one control period".), said control means (processor and timing sections 35 and 27) defining a single detection area (central focusing area 66) which is both vertically and horizontally limited within said imaging device (The total image detection area 66 and 68 of image sensor 20 is limited by the left/right and top/bottom edges of the sensor; As shown in figure 1, the central focusing area 66 is within those bounds.) and reading only the image signals within the single detection area out (66) of said imaging device (During a focusing operation, Parulski et al. only reads out signal charges within the central focusing area 66 and dumps the rest of the charges using the "fast flush"; see figure 9), the read image signals being used to adjust the still image before photographing ("Integrate Final Image" step") and a control period ("non-used lines are quickly flushed") of said control means being set in correspondence within a read-out period ("fast flush") associated with said single detection area (see column 5, lines 54 – 66; and also see explanation below).

As shown in figure 4, "only a small number lines in- the central focusing area 66 of the image are used to provide the focus determination input data." As shown in figure 5, "the average contrast could be computed for a center region 80, a left central region 82, and the right

central region 84." In figure 4, the detection area is vertically limited to a small number of lines and horizontally limited by the pixel plane (as in Applicant's figure 4) and further, in figure 5, the detection area is vertically limited to a small number of lines and horizontally limited to central regions.

On column 8 (line 39) – column 9 (line 9), Parulski et al. indicates that the AF mode lasts for an indefinite period of time and after that indefinite period of time a final image is then integrated. More specifically, Parulski et al. states, "the process of integrating and reading out the focus image is then repeated – numerous times as the lens focus is adjusted until it provides the maximum average contrast – the focus is acceptable." Therefore, the control means cannot integrate the final image until the focus is acceptable – i.e. the control means control period switchover (from AF period to still image capture period) is determined by the read-out period of the detection area.

Finally, while Parulski et al. indicate that the central focusing area (66) is located at a central area of an effective pixel plane, it is read-out according to the line-skipping patterns of figures 10 and 11. Parulski et al. further indicate that to read-out in such a pattern, the sensor timing circuit (28) operates according the timing diagram shown in figure 12. Parulski et al., also state in column 8 (lines 1 – 5), "the advantage … [is] to reduce the amount of data that must be handled from the central focusing area 66". Parulski et al. additionally indicate (see column 5, lines 54 – 66) that, "non-used lines are quickly flushed".

While Parulski et al. disclose that the image signals associated with the single detection area (66) are used for automatic focus control, and more particularly, that a high frequency component of the image signals are used for AF control. However, Parulski et al. do not further

specify that a luminance signal associated with the single detection area is used for an automatic photographic sensitivity control and a chrominance signal associated with the single detection area is used for an automatic white balance control or wherein the single detection area includes only horizontal lines.

On the other hand, Kijima et al. disclose an image photographing apparatus and method of operating thereof for reading out a single detection area within the image sensor. Kijima et al. specifically show, in figures 1 and 6, an image sensor (13) and a control means (17) for reading out the single detection area ("effective area"). Kijima et al. further teach, as stated in column 10 (line 52) – column 11 (line 17), wherein the image signals within the single detection area ("effective area") are used for auto-focusing control, auto-exposure control, and auto-white-balance control. Kijima et al. further disclose wherein the single detection area includes only consecutive horizontal lines (see column 10, lines 52 – 64). While not specifically stated in Kijima et al., it necessary to evaluate the luminance signals and chrominance signals of the image signals associated with the single detection area ("effective area") to perform the stated auto-exposure and auto-white-balance control.

Hence, at the time the invention was made, it would have been obvious to one with ordinary skill in the art to have further used the image signals within the single detection area for auto-focusing control, auto-exposure control, and auto-white-balance control (as taught by Kijima et al.) in the image photographing apparatus (disclosed by Parulski et al.) for the advantage of producing a high-quality image.

While Parulski et al. and Kijima et al. each disclose a timing control section (27 and 17, respectively); the particulars of the sensor timing circuit (28/17) or the control interface (52 and

18, respectively) are not disclosed. Accordingly, Parulski et al. and Kijima et al. do not teach a frequency dividing means for generating and outputting a normal vertical clock for reading out the image signals and a high speed clock having a higher frequency than that of the normal vertical clock; a pulse counter circuit for receiving instructions from said control means indicating a quantity of rows that are read using a high speed clock and setting a value in response to the quantity of rows, wherein when the quantity of rows equals a predetermined value of counted rows, output signals are generated to control a switching unit which switches from the high speed clock to a normal vertical clock.

On the other hand, Nishizawa et al. also disclose an image photographing apparatus and method of operating thereof for reading out a single detection area within the image sensor. Nishizawa et al. specifically show, in figures 5 and 8A, an image sensor (CHI) and a control means (collectively clock pulse generator CPG and registers reg2 and reg1) for reading out the single detection area ("valid" region). Nishizawa et al. further teach, as stated in column 10 (lines 1 – 63), a pulse counter circuit (collectively pulse counter CT and comparators cmp2 and cmp1) receiving instructions ("REG1 stores a constant vi … a comparator CMP1 compares and stores the relation between the levels … of REG1 and the counter CT; see column 10, lines 20 – 32) from said control means (REG1 is part of the control means) indicating a quantity of rows that are not to be read out and are read using a high speed clock ("since the gates … are open until the value of the counter CT takes 121, the vertical scanning register Vreg is derive at a high speed"; see column 10, lines 33 – 39) and setting a value in response to the quantity of rows that are not to be read out ("the logic [from the comparator CMP1] is inverted to '0'"; see column 10, line 34).

Nishizawa et al. further, as also stated in column 10 (lines 20 – 34), teach wherein when the quantity of rows that are not to be read out ("the value of the counter CT … ") equals a predetermined value of counted rows ("… takes 121"), output signals are generated to control a switching unit which switches from the high speed clock to a normal vertical clock ("the value of the counter CT takes 121, the vertical scanning register Vreg is driven at a high speed by the horizontal scanning clock signals H1 and H2 and after the 122-th vertical scanning by the ordinary vertical scanning clock signals V1 and V2"; also see column 10, lines 56 – 57) and, accordingly, "the normal vertical clock corresponds to a read out period where horizontal lines corresponding to the detection area are read out." Finally, Nishizawa et al. give clear indication that the clock pulse generator (CPG) is a frequency dividing means that generates and outputs a normal vertical clock for reading out the image signals and a high speed clock having a higher frequency than that of the normal vertical clock. See column 7 (lines 13-26).

Therefore, at the time the invention was made, it would have obvious to one with ordinary skill in the art to have included the pulse counter circuit for receiving instructions indicating a quantity of rows that are read using a high speed clock and when the quantity of rows equals a predetermined value of counted rows, output signals are generated to control a switching unit which switches from the high speed clock to a normal vertical clock (as taught by Nishizawa et al.) in the image photographing apparatus and corresponding method of operating thereof for only reading image signals within a single detection area (taught by Parulski et al. in combination with Kijima et al.) for the advantage of providing *a solid state image pickup apparatus for exclusive use (e.g., pattern recognition with a narrow image pickup range) capable of high-speed operation* (see Nishizawa et al.; column 1, lines 26 – 36).

8. For **Claims 11 and 16**, Parulski et al. disclose, as shown in figures 1, 4, 5, 8, and 9 and as stated in columns 4 (lines 49 – 59), 5 (lines 54 – 67), 6 (lines 1 – 14, 19 – 22, and 26 – 33), 8 (lines 6 – 67), and 9 (lines 1 – 8), an image photographing apparatus and method of operating thereof for photographing a still image, comprising:

a scanning imaging device (sensor 20; see figures 1 and 4) for generating image signals; and

a control means (processor section 35 and timing control section 27; see figure 1) for using the image signals generated by said imaging device (sensor 20) to adjust the still image during at least one control period before photographing (As shown in figure 9, the claimed "photographing" is in the step "Integrate Final Image"; the claimed "adjust the still image" corresponds to all the steps prior to the "Integrate Final Image Step"; one iteration of the "Focus Acceptable" loop corresponds to the claimed "at least one control period".), said control means (processor and timing sections 35 and 27) defining a single detection area (central focusing area 66) which is both vertically and horizontally limited within said imaging device (The total image detection area 66 and 68 of image sensor 20 is limited by the left/right and top/bottom edges of the sensor; As shown in figure 1, the central focusing area 66 is within those bounds.) and reading only the image signals within the single detection area out (66) of said imaging device (During a focusing operation, Parulski et al. only reads out signal charges within the central focusing area 66 and dumps the rest of the charges using the "fast flush"; see figure 9), the read image signals being used to adjust the still image before photographing ("Integrate Final Image" step").

As shown in figure 4, "only a small number lines in- the central focusing area 66 of the image are used to provide the focus determination input data." As shown in figure 5, "the average contrast could be computed for a center region 80, a left central region 82, and the right central region 84." In figure 4, the detection area is vertically limited to a small number of lines and horizontally limited by the pixel plane (as in Applicant's figure 4) and further, in figure 5, the detection area is vertically limited to a small number of lines and horizontally limited to central regions.

On column 8 (line 39) – column 9 (line 9), Parulski et al. indicates that the AF mode lasts for an indefinite period of time and after that indefinite period of time a final image is then integrated. More specifically, Parulski et al. states, "the process of integrating and reading out the focus image is then repeated – numerous times as the lens focus is adjusted until it provides the maximum average contrast – the focus is acceptable." Therefore, the control means cannot integrate the final image until the focus is acceptable – i.e. the control means control period switchover (from AF period to still image capture period) is determined by the read-out period of the detection area.

Finally, while Parulski et al. indicate that the central focusing area (66) is located at a central area of an effective pixel plane, it is read-out according to the line-skipping patterns of figures 10 and 11. Parulski et al. further indicate that to read-out in such a pattern, the sensor timing circuit (28) operates according the timing diagram shown in figure 12. Parulski et al., also state in column 8 (lines 1 – 5), "the advantage … [is] to reduce the amount of data that must be handled from the central focusing area 66". Parulski et al. additionally indicate (see column 5, lines 54 – 66) that, "non-used lines are quickly flushed".

While Parulski et al. disclose that the image signals associated with the single detection area (66) are used for automatic focus control, and more particularly, that a high frequency component of the image signals are used for AF control. However, Parulski et al. do not further specify that a luminance signal associated with the single detection area is used for an automatic photographic sensitivity control and a chrominance signal associated with the single detection area is used for an automatic white balance control or wherein the single detection area includes only horizontal lines.

On the other hand, Kijima et al. disclose an image photographing apparatus and method of operating thereof for reading out a single detection area within the image sensor. Kijima et al. specifically show, in figures 1 and 6, an image sensor (13) and a control means (17) for reading out the single detection area ("effective area"). Kijima et al. further teach, as stated in column 10 (line 52) – column 11 (line 17), wherein the image signals within the single detection area ("effective area") are used for auto-focusing control, auto-exposure control, and auto-white-balance control. Kijima et al. further disclose wherein the single detection area includes only consecutive horizontal lines (see column 10, lines 52 – 64). While not specifically stated in Kijima et al., it necessary to evaluate the luminance signals and chrominance signals of the image signals associated with the single detection area ("effective area") to perform the stated auto-exposure and auto-white-balance control.

Hence, at the time the invention was made, it would have been obvious to one with ordinary skill in the art to have further used the image signals within the single detection area for auto-focusing control, auto-exposure control, and auto-white-balance control (as taught by

Kijima et al.) in the image photographing apparatus (disclosed by Parulski et al.) for the advantage of producing a high-quality image.

While Parulski et al. and Kijima et al. each disclose a timing control section (27 and 17, respectively); the particulars of the sensor timing circuit (28/17) or the control interface (52 and 18, respectively) are not disclosed. Accordingly, Parulski et al. do not teach wherein the control means controls at least two scan speeds with a first scan speed being used outside the single detection area and a second scan speed being used within the single detection area, the first scan speed being greater than the second scan speed; and a pulse counter circuit for receiving instructions from said control means indicating a quantity of rows that are read using a high speed clock and setting a value in response to the quantity of rows, wherein when the quantity of rows equals a predetermined value of counted rows, output signals are generated to control a switching unit which switches from the high speed clock to a normal vertical clock.

On the other hand, Nishizawa et al. also disclose an image photographing apparatus and method of operating thereof for reading out a single detection area within the image sensor. Nishizawa et al. specifically show, in figures 5 and 8A, an image sensor (CHI) and a control means (collectively clock pulse generator CPG and registers reg2 and reg1) for reading out the single detection area ("valid" region). Nishizawa et al. further teach, as stated in column 10 (lines 1 – 63), a pulse counter circuit (collectively pulse counter CT and comparators cmp2 and cmp1) receiving instructions ("REG1 stores a constant vi … a comparator CMP1 compares and stores the relation between the levels … of REG1 and the counter CT; see column 10, lines 20 – 32) from said control means (REG1 is part of the control means) indicating a quantity of rows that are not to be read out and are read using a high speed clock ("since the gates … are open

until the value of the counter CT takes 121, the vertical scanning register Vreg is derive at a high speed"; see column 10, lines 33 – 39) and setting a value in response to the quantity of rows that are not to be read out ("the logic [from the comparator CMP1] is inverted to '0'"; see column 10, line 34).

Nishizawa et al. further, as also stated in column 10 (lines 20 – 34), teach wherein when the quantity of rows ("the value of the counter CT … ") equals a predetermined value of counted rows that are not to be read out ("… takes 121"), output signals are generated to control a switching unit which switches from the high speed clock to a normal vertical clock ("the value of the counter CT takes 121, the vertical scanning register Vreg is driven at a high speed by the horizontal scanning clock signals H1 and H2 and after the 122-th vertical scanning by the ordinary vertical scanning clock signals V1 and V2"; also see column 10, lines 56 – 57). Finally, Nishizawa et al. give clear indication that the clock pulse generator (CPG) is a frequency dividing means that generates and outputs a normal vertical clock for reading out the image signals and a high speed clock having a higher frequency than that of the normal vertical clock. See column 7 (lines 13-26).

Therefore, Nishizawa et al. wherein the control means (CPG; REG1 and REG2) controls at least two scan speeds with a first scan speed ("high speed") being used outside the single detection area (up to count value 121) and a second scan speed ("ordinary vertical clock scanning signals") being used within the single detection area, the first scan speed being greater than the second scan speed and, accordingly, "the normal vertical clock corresponds to a read out period where horizontal lines corresponding to the detection area are read out.

Therefore, at the time the invention was made, it would have obvious to one with

ordinary skill in the art to have included the pulse counter circuit for receiving instructions indicating a quantity of rows that are read using a high speed clock and when the quantity of rows equals a predetermined value of counted rows, output signals are generated to control a switching unit which switches from the high speed clock to a normal vertical clock (as taught by Nishizawa et al.) in the image photographing apparatus and corresponding method of operating thereof for only reading image signals within a single detection area (taught in combination by Parulski et al. and Kijima et al.) for the advantage of providing *a solid state image pickup apparatus for exclusive use (e.g., pattern recognition with a narrow image pickup range) capable of high-speed operation* (see Nishizawa et al.; column 1, lines 26 – 36).

9. As for **Claims 2, 7, 12, and 17**, Parulski et al. disclose wherein said control means (processor section 35 and timing control section 27) also controls said imaging device (sensor 20) when the still image is being photographed.

Parulski et al. states, in column 4 (lines 28 – 39), "The output of the image sensor 20 is amplified and processed in an analog gain and sampling (correlated double sampling (CDS)) circuit 32, and converted to digital form in A/D converter 34. The A/D output signal is provided to a processor section 35, which includes a digital processor 36 which temporarily stores the still images in a DRAM memory 38. The digital processor 36 then perform image processing on the still images, and finally stores the processed images on the removable memory card 26 via a memory card interface circuit 40, which may use the PCMCIA 2.0 standard interface. An EPROM memory 42 is used to store the firmware which operates the digital processor 36."

10. As for **Claims 3, 8, 13, and 18**, Parulski et al. disclose wherein said control means (processor section 35 and timing control section 27) determines a start position of the single

detection area (central focus area 66) and the amount of image to be read out within the single detection area, and, accordingly, only the image signals within the single detection area (central focus area 66) are read out of the said imaging device (sensor 20).

Parulski et al. states, in column 4 (lines 22 – 28), "Control of the sensor 20 is provided by a timing and control section 27, which specifically includes a sensor timing circuit 28. The sensor timing circuit 28 provides the signals to enable sensor drivers 30, which provides horizontal clocks (H1, H2) and vertical clocks (V1, V2), as well as a signal FDG for activating a drain structure on the sensor 20."

Furthermore, Parulski et al. states, in column 6 (lines 26 – 34), "In the autofocus mode, the timing and control section 27 controls the fast dump structure 62 to A) eliminate all lines of image charge in the outer area 68 (FIG. 4) outside the central focusing area 66, and B) eliminate at least one line of image charge from the image sensor 20 for every one or more lines of image charge that are transferred to the horizontal register 60 for readout from the central focusing area 66."

11. As for **Claims 4, 9, 14, and 19**, as stated above, Nishizawa et al. further, as also stated in column 10 (lines 20 – 34), teach wherein when the quantity of rows ("the value of the counter CT … ") equals a predetermined value of counted rows ("… takes 121"), output signals are generated to control a switching unit which switches from the high speed clock to a normal vertical clock ("the value of the counter CT takes 121, the vertical scanning register Vreg is driven at a high speed by the horizontal scanning clock signals H1 and H2 and after the 122-th vertical scanning by the ordinary vertical scanning clock signals V1 and V2"; also see column 10, lines 56 – 57). Therefore, Nishizawa et al. wherein the control means (CPG; REG1 and

REG2) controls at least two scan speeds with a first scan speed ("high speed") being used outside the single detection area (up to count value 121) and a second scan speed ("ordinary vertical clock scanning signals") being used within the single detection area, the first scan speed being greater than the second scan speed.

Therefore, Nishizawa et al. disclose a high-speed scan in a region before the start position of the single detection area, allows a predetermined-speed scan in the single detection area, and allows only the determined amount of image signals to be read out.

12. As for **Claims 5, 10, 15, and 20**, Parulski et al. disclose wherein, based on the read image signals, at least one of automatic focus control, automatic photographic sensitivity control, and automatic white balance control is performed.

Parulski et al. performs automatic focus control on the read image signals (see figure 9).

Conclusion

13. Any inquiry concerning this communication or earlier communications from the Examiner should be directed to Justin P Misleh whose telephone number is 571.272.7313. The Examiner can normally be reached on Monday through Friday from 8:00 AM to 5:00 PM.

If attempts to reach the Examiner by telephone are unsuccessful, the Examiner's supervisor, David Ometz can be reached on 571.272.7593. The fax phone number for the organization where this application or proceeding is assigned is 571.273.8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished

applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

/Justin P. Misleh/
Primary Examiner
Group Art Unit 2622
December 3, 2008